International Journal of Reconfigurable and Embedded Systems
Vol. 7, No. 3, November 2018, pp. 166~172
ISSN: 2089-4864, DOI: 10.11591/ijres.v7.i3.pp166-172

Design Considerations of Reconfigurable CMOS Mixers for Multi-standard Communication Receiver Systems

Manoj Kumar Vishnoi, Satya Sai Srikant
Department of Electronics and Communication Engineering, SRM Institute of Science and Technology India

Article Info

Article history:

Received Aug 11, 2018
Revised Oct 12 , 2018
Accepted Oct 26, 2018

Keywords:

Active mixers
Multi-standard receivers
Reconfigurable
Tow thomas bi-quad topology
Wide-band

ABSTRACT

This paper has been carried out the study of reconfigurable wide-band mixers that can do the frequency conversion and gain variation standards with low noise and high linearity used in multi-mode and multi-standard receivers. Over the last few years reconfigurability has become very popular in adopting technology to meet the wideband wireless communication specifications that is compatible with multi-standards like GPS (1.57 GHz), WLAN (2.4 GHz-5.9 GHz), Bluetooth (2.402–2.483 GHz) and ZigBee (0.784-0.915 GHz) in low power consumption environment. The reconfigurability can be achieved between low and high band modes through power switching in RF frequency mixers. It can be achieved by flipping the input RF signal between gate and source terminal of input transistor and altering the trans-impedance stage output. With the concept of reconfigurable transistor pair with open and short circuit stubs, one can not only find the configurable gain with center frequencies 7.355, 8.65, 11.35 and 12.65 GHz but also with high power efficiency. Tow Thomas Bi-Quad Topology other than the traditional current commuting technique for the second order trans-impedance amplifier stage, works as a current mode filter over a tunable bandwidth. The active Gilbert mixers are used widely in most of communication system, due to its significance gain, perfect isolation, and linearity in response.

Corresponding Author:

Manoj Kumar Vishnoi,
Department of Electronics and Communication Engineering,
SRM Institute of Science and Technology
Delhi NCR Campus Ghaziabad, 201204, India
Email: manojvishnoi.vlsi@gmail.com

1. INTRODUCTION

The highly growth in wireless satellite communication, optical communication and military application with internet platform has made tremendous demand for low cost, low power and high performance multimedia, multi-standard transceivers. The system having Wi-Fi, Ultra Wideband, Bluetooth, ZigBee, Internet of things (IOT) enabled platform and cognitive interface with sophisticated performance, endless connectivity, demands the reconfigurable smart mixers. The mixer, a major building block in transmitter/receiver, affects the overall performance of the communication system, having three port non-linear circuit is used to convert the radiofrequency signal up or down to an intermediate frequency signal. A high frequency mixer can reduce the gain, while a high linearity mixer can increase the overall system linearity and its dynamic range [1]. If a mixer increase the frequency to $f_{RF}+f_{LO;}$ then the mixer is an up-convertor mixer, on the other hand if the frequency is decreased to $f_{RF}-f_{LO}$; the mixer is called a down-convertor mixer, where the f_{RF} andf_{LO} are the frequencies of incoming signal and local oscillator. While analyzing the performance of a mixer, the various specifications like conversion gain, noise figure, flicker noise (1/f), linearity, 1dB compression point and interception point are taken for consideration. CMOS device circuits have now been scaled down to reduce the channel length for achieving the sharpened radio

frequency performance, but with extra flicker noise [2]. The flicker noise is reduced by using PMOS switching technique, to alter the height and width of noise pulse [3]. By emplacing the currents to input stage and switching stage individually other than a traditional methods of providing similar current to both stages, leads to optimization of gain and total noise contribution including flicker noise [4]. A passive mixer for television tuner operating at 48 to 860 MHz can achieve the gain of 19.5 dB with zero flicker noise [5]. To design the radio frequency reconfigurable wireless communication system, researchers have introduced the RF transceiver with mixer having flexible frequency bandwidth and conversion gain variation. A CMOS quadrature demodulator receiver provides the reconfigurability in terms of frequency variation at wide range applicable for GSM/DCS/CDMA cellular standards in multimode communication system [6]. Also an inductor-less variable range receiver have been introduced to palliate the effect of jammer on different bands signals [7]. The variable mixer with double balanced Gilbert cell [8] and CMOS folded switching mixer [9] working in 3-5 GHZ band can produce an adjustable transition gain for multiband OFDM (MB-OFDM) UWB standard. Most of proposed reconfigurable mixers have shown gain variant conversion and bandwidth tuning through current variation, load tuning etc.Recent work on variable gain conversion mixersmakes it possible for designing reconfigurable system to approach the gain controllability [10-13].

2. RECONFIGURABLE MIXER DESIGN TECHNIQUES

The communication systems with multimode and multi-standard configurability are designed for reconfiguration between active and passive mode with gain and frequency with low noise occurrence. The system gives the high conversion gain, low noise figure, moderate linearity but high power consumption in active mode, while in passive mode low conversion gain, low flicker noise with better linearity and low power consumption.

The Nisha Gupta et al [15-16], proposed a reconfigurable down conversion mixer with adjustable gain and bandwidth through current distribution between input and switching stages, and altering the load output. A fully differential RF input impedance of 50 Ω is usually considered in order to eliminate the common mode noise and second harmonics. It is achieved by converting RF input voltage into RF current, to get commutated with switches stage and then passing on to first order low pass filtering circuit shown in Figure 1. The higher IIP3 with same bias current and high band transconductance (g_m) can be achieve to work from 0.6–5 GHz by using multi-gated input pair of transistors. To minimize the current and parasitic capacitance to a least possible value at the transconductance output, thereby increasing the output impedance to a high level; so that reducing the overall noise, the common mode voltage is set to $V_{DD}/2$.

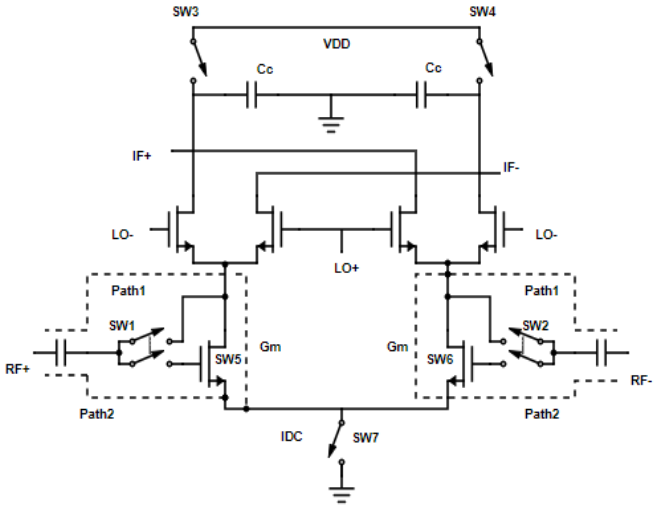

Figure 1. Wideband reconfigurable mixer

The switching stage changes the circuit configuration to work in active or passive mode by flipping the load. In passive mode, the mixer is simply combination of four transistors working as degeneration resistor and switches to increase the linearity, while capacitor C_C to suppress the noise at higher frequency [17].

In active mode configuration, the common source topology in double balanced Gilbert cell architecture provide the current, flowing through Mn1 and Mn2 (S_W 5-6) switches with different selection of bias voltage to control the parameters of transconductance stage, so as to achieve the variation in high gain and low noise figure. The high linearity is achieved by providing the zero voltage to g_m stage through virtual ground at trans-impedance amplifier stage.

A two stage miller compensated OTA topology having output transconductance amplifier with feedback R_F, C_F is opted for obtaining output undulation at high peak and input attributed noise at low level to design a trans-impedance amplifier, that convert the input current to voltage output, serving as a load and anti-aliasing filter in passive mode. In active mode configuration, to save the power TIA is being switched off.

Ming Wang and Carlos E. Saavedra [18] discovered a down-converter Gilbert cell mixer, in which the conversion gain can be varied by doing restyle of total gate width (W) of transistor devices other than the traditional variable gain amplifier and attenuator. In this architecture three transistors in left side and three transistors in right side are used in RF transconductance stage of the mixer in parallel to accomplish two disengage tasks of gain curtailment and frequency transformation simultaneously, which lead to reduce the chip area. This reconfigurable mixer shown in Figure 2 can provide the conversion gain from 9 dB consuming 2.4 mW to 24 dB with 18 mW, power consumption.

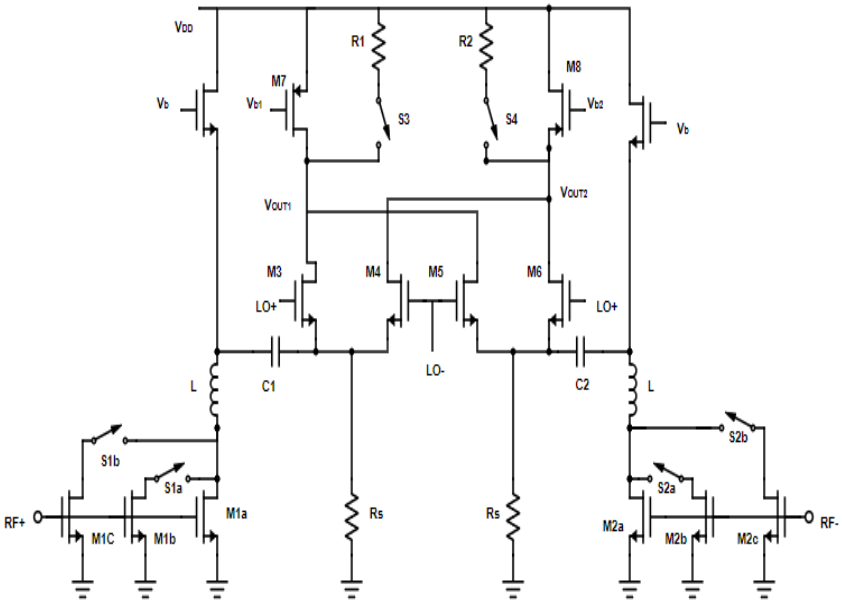

Figure 2. Reconfigurable Gilbert cell broadband

This down-converter mixer has individual dc biased current for RF transconductance stage and Local Oscillator switching core to optimize the conversion gain and reduce the overall noise performance. The output is taken at the notch of inductor and load, to obtain the inductive peaking impact 40%, on the amount of broadband extension, approaching the broadband frequency response ranging from 2-10 GHz, regardless of conventional shunt peaking technique. In this the output is at the intersection of amplifying transistor and peaking inductor. The gate width of circuit having three parallel devices in both the left hand side and right hand side with four switches M1b, M1c, M2b and M2cconnected to transistors in ON condition is given by

$$W_{tot}=W_a+W_b+W_c$$

Where W_a, W_b and W_c are gate-width of transistors M_{1a} M_{1b} M_{1c} and M_{2a} M_{2b} M_{2c} respectively. The overall conversion gain of the RF circuit in saturation can be calculated as:

$$CG=2/\pi\ v_{sat}C_{ox}\ Z_L\ [W_a+W_b+W_c]$$

The conversion gain of mixer is varied in accordance with transistor gate-width variation having different combination of switches in ON/OFF condition.

Zhangf Liu, Jing Wang proposed a reconfigurable mixer [19] compromise of double balanced Gilbert cell mixer and reconfigurable matching network which is being used in USA GPS and China Beidou receiver system. This RF integrated circuit a single chip circuit is capable of achieving the reconfiguration function of GNSS receiver. The mixer shown in Figure 3 is designed on 0.18 micrometer CMOS process. The reconfigurable matching network has software definable MOS switches S_{W1}, S_{W2} S_{W3} and S_{W4} shown in Figure 3.

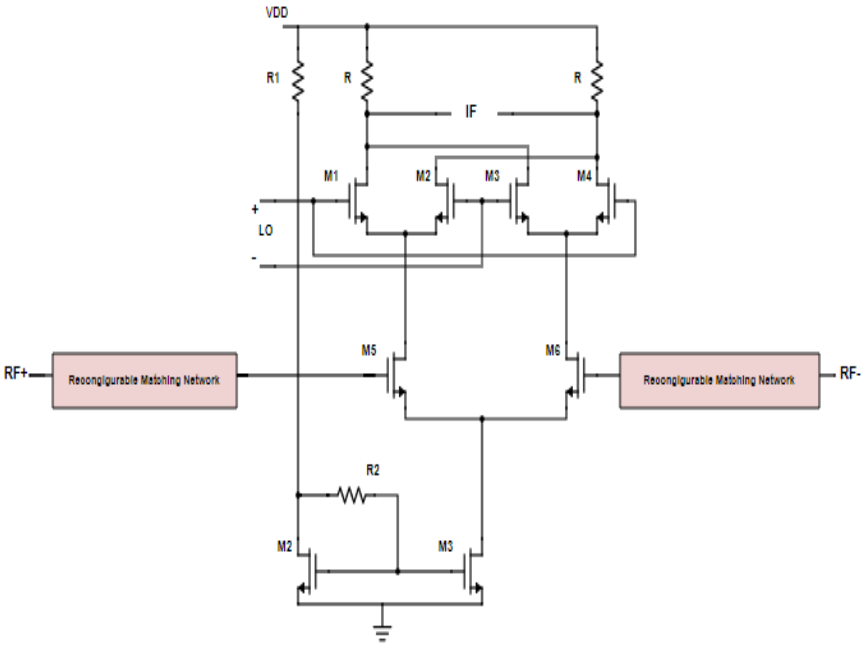

Figure 3. Reconfigurable double balanced Gilbert cell mixer

When the switches S_{W1},S_{W2}, $S_{W3}$and S_{W4} are in the different combination of "on" and "off" conditionwith L_1, L_2, C_1 and C_2 series and parallel connection, the matching network make different structure to approach the frequency configuration for GPS and Beidou.

Chiu et al. [20-21] rediscovered a self-oscillating mixer, comprises of an active mixer and oscillator, to produce the frequency transition at centre frequency 7.35, 8.65, 11.35 and 12.65 GHz with a conversion gain providing variation from 7.83dB to 18.7 dB. The self-oscillating mixer circuit is made in a reconfigurable transistor topology for a less cost, high efficient and stable bias front end receiver. Sub-harmonic self-oscillating mixer as shown in Figure 4.

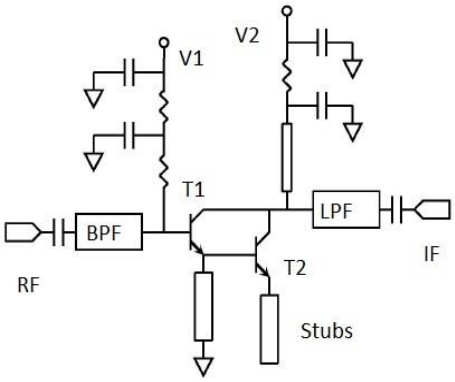

Figure 4. Sub-harmonic self-oscillating mixer

The circuit shown in Figure 4 consist of a band pass filter playing a role of DC block capacitor and resonator, that make oscillation between band pass filter and transistor T1, tends to a self-oscillating operation, sixth order Butterworth response low pass filter to subdue the high frequency components, local radio frequency, image and spurious signal, and dual bias network with different biased transistors T1 and T2 to achieve the frequency and gain conversion. The band pass filter is a Chebyshev BPF has a small insertion loss. The transistor T1 is biased for oscillation in class AB operation of the common emitter configuration and T2 is biased with zero base emitter voltage to serve as an auxiliary oscillator to provide the stable oscillation for T1. The capacitor at base emitter of T2 and open circuit stub working as a return path for the RF signal, make the series feedback of the common emitter oscillation of T1 to generate the local oscillator signal and its harmonics mix with the RF within T1. The IF signals are taken out from the low pass filter.

Laleh Rabieirad and Saeed Mohammadi [22] presented a programmable in dual mode having three stages distributed amplifier/mixer consist of transistor switches, low loss transmission line and RF transistors. These are combined to achieve functional reconfigurability using 1 bit programmable signal. The circuit shown in Figure 5 provides a gain of 8 dB in 3-8 GHz bandwidth in distributed amplifier mode, while in distributed mixer mode; the average conversion gain is 4 DB in a 1-16 GHZ bandwidth.

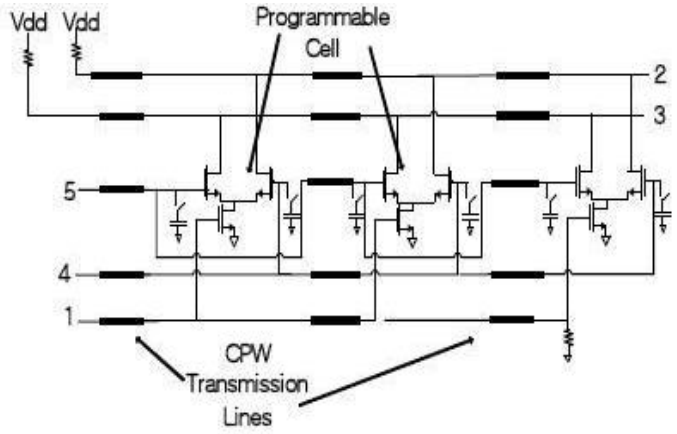

Figure 5. Schematic of distributed programmable amplifier/mixer

The CMOS transistor switches are used for low insertion loss in on state and isolation in off state, which are employed to couple and decouple RF transmission lines from the signal path. The RF block is a two incorporated cascode cell having two transistors constructing a differential pair to operate with same signal amplitude and phase in amplifier mode. In distributed mixer mode these transistors functional companion as a switch pair with transconductance stage.

Mirko Pasca et al.[23- 26] presented a highly linear, low power 12 dBm IIP3 reconfigurable mixer for impulse radio ultra wideband receiver. This mixer are being used in various applications like, sensor networking and short range communication system because of low power consumption and high operating frequency. This down-conversion mixer is design to reconfigured for different channels, in low band (Channel 3 consists4.4928 GHz carrier with 499.2 MHz channel bandwidth), in high band (Channel 9 consists7.9872 GHz carrier with 499.2 MHz channel bandwidth and Channel 11 consists, 7.9872GHz carrier with 1.331 GHz channel bandwidth). The high linearity is achieved using derivative superposition method and source degeneration input stage as shown in Figure 6. The mixer consists of a Gilbert switching stage and source degeneration RF input stage to reduce voltage drop across load resistors, achieving high output signal swing and high linearity.

The transistors M_1, M_2, M_3, M_4 and resistors R_5, R_6, R_7, R_8 and ON-OFF switches M_{14}, M_{15} are used to make source degenerated input stage with CMOS amplifier to achieve high gain and linearity acquiring second order distortion cancellation. To improve third-order intercept point (IIP3) performance by cancelling order non-linear current, the transistors M_1 and M_3 are biased in weak inversion region [27-29]. To emphasize conversion gain and to cut-down parasitic capacitances, the inductor L_1 is placed between RF input stage, limiting load resistors. The transistors M_{12}, M_{13}, M16, and M17 enable/disable capacitances C_9 and C_{10} for the modification of resonance frequency that can be operated in lower or upper band in infrared – ultra wide band (IR-UWB). The resistors R_1, R_2, R_3 and R4 provide parallel switchable connection to acquire

variable conversion gain for different frequencies and capacitors C_1, C_2 C_3 and C_4 are connected to eliminate the DC component at the input stage.

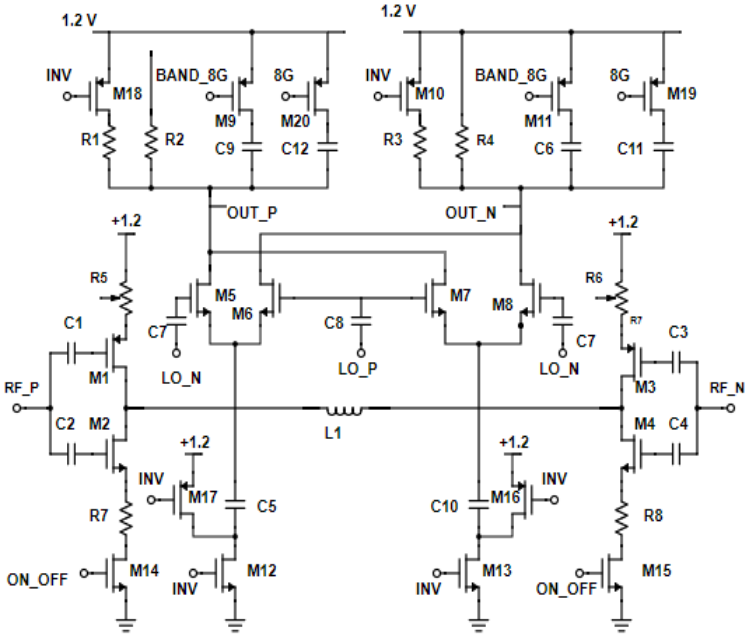

Figure 6. Reconfigurable Mixer Schematic

4. CONCLUSION

This paper has described the study of wideband multimode mixers that can be used to perform the multiple task of frequency conversion and gain control simultaneously presented by various researchers. To enhance the trans-conductance's efficiency and reducing the 1/f flicker noise, a differential complimentary pair of transistor was used. Multiband sub-harmonic self-oscillating mixer was designed to achieve high performance conversion gain using reconfigurable transistor pair for microwave and millimeter baseband circuits. In RF trans-conductor stage, the size effective gate width of the devices can be reconfigured by placing parallel transistors and switches to change conversion gain. Derivative superposition method with source degeneration input stage can achieve high gain with different channel bandwidth for sensor network and high operating frequency system. To acquire the high linearity, source degeneration and tuning techniques with a little contribution of noise figure has been introduced in Gilbert cell mixer. Finally we conclude that, a fully differentially pair of transistors at the RF input to eliminate the second harmonics by converting RF input voltage into RF current to get commutated with switches stage for the reconfiguration strategies and design techniques in a very sophisticated manner for wireless applications.

ACKNOWLEDGEMENTS

The authors would like to thanks Dr. P.K. Chaturvedi from SRM Institute of Science and Technology for their technical guidance and support. We would appreciate all the referred authors from where we have taken the details of reconfigurable power amplifiers

REFERENCES

[1] Mengxiong Li ; Barrie Hayes-Gill ; Matt Clark ; Mark Pitter ; Mike Somekh ; Ian Harrison,"5-GHz optical front-end for active pixel applications in standard 0.35-µm CMOS" SPIE 6477, Silicon Photonics II,647708 February 09, 2007

[2] B. Razavi, "Design considerations for direct-conversion receivers", IEEE Trans. Circuits Syst. II, Analog Digital Signal Process., vol. 44, no. 6, pp. 428-435, Jun. 1997.

[3] D. Manstretta et al., "Low 1/f Noise CMOS Active Mixers for Direct Conversion", IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process. vol. 48, no. 9, pp. 846-850, Sep. 2001.

[4] H. Darabi, J. Chiu, "A noise cancellation technique in active RF-CMOS Mixers", IEEE J. Solid-State Circuits, vol. 40, no. 12, pp. 2628-2632, Dec. 2005.

[5] Viet-Hoang Le; Hoai-Nam Nguyen; In-Young Lee; Seok-Kyun Han; Sang-Gug Lee, "A Passive Mixer for a Wideband TV Tuner," Circuits and Systems II: Express Briefs, IEEE Transactions on,vol.58, no.7,pp.398,401, July 2011
[6] Poobuapheun, N.; Wei-Hung Chen; Boos, Z.; Niknejad, A.M.,"A 1.5V 0.7-2.5GHz CMOS Quadrature Demodulator for Multi-Band Direct-Conversion Receivers," Custom Integrated Circuits Conference (CICC '06) IEEE, pp.797-800, Sept. 2006.
[7] Poobuapheun, N.; Wei-Hung Chen; Boos, Z.; Niknejad, A.M., "An inductorless high dynamic range 0.3 2.6 GHz receiver CMOS frontend," Radio Frequency Integrated Circuits Symposium (RFIC 2009) IEEE , pp.387-390, June 2009
[8] Hong Zhang; Guican Chen; Xiao Yang, "Fully Differential CMOS LNA and Down-Conversion Mixer for 3-5 GHz MB-OFDM UWB Receivers," Radio-Frequency Integration Technology (RFIT 007). Pp.54-57, Dec. 2007.
[9] H.-Y. Wang, K. F. Wei, J.-S. Lin, and H. R. Chuang, "A 1.2-V Low LO-Power 3-5 GHz Broadband CMOS Folded-Switching Mixer for UWB Receiver," in Radio Frequency Integrated Circuits Symposium, 2008. RFIC 2008. IEEE, pp. 621–624, 17 2008-April 17.
[10] R. Circa, D. Pienkowski, G. Bck, and R. Wittmann," Reconfigurable UMTS/WLAN RF receiver, in Proc. 3rd Software Radios Workshop, Karlsruhe, Germany, Mar. 2004, pp. 6571.
[11] Kakerow, R.; Mueller, M.; Pienkowski, D.; Circa, R.; Boeck, G., "Reconfigurable receiver approach for 4G terminals and beyond," IEEENEWCAS Conference, 2005. The 3rd International, pp.9-12, June 2005.
[12] Chong-Ru Wu, Hsieh-Hung Hsieh, Li-Shin Lai, and Liang-Hung Lu, "A 3–5 GHz Frequency-Tunable Receiver Frontend for Multiband Applications" IEEE Microwave and Wireless Components Letters, Vol. 18, No. 9, September 2008.
[13] A. Costantini, A. Pezzotta, A. Baschirotto, M. De Matteis, S. D'Amico, F. Murtas, G. Gorini, "A CMOS 0.13um Low Power Front-end for GEM Detectors," in 19th IEEE International Conference on Electronics, Circuits and Systems (ICECS), pp. 193–196, Jan. 2012.
[14] C.-H. Wu and H.-T. Chou, "A 1.2-V High-Gain UWB Mixer Utilizing Current Mirror Topology," in Ultra-Wideband (ICUWB), 2010 IEEE International Conference on, vol. 1, pp. 1–4, Sept.
[15] Nish Gupta, Ashudev Dutta and Shiv Govind Singh, "A Low/High Band Highly Linearized Reconfigurable Down Conversion Mixer in 65nm CMOS Process" Nordic Circuits and Systems Conference (NORCAS): NORCHIP & International Symposium on System-on-Chip (SOC), 2015
[16] Kuan Bao, Xiangning Fan, Li Tang, Zaijun Hua, and Zhigong Wang "A CMOS Reconfigurable Passive Mixer with Digitally-Controllable Gain" Radio-Frequency Integration Technology (RFIT), 2014 IEEE International Symposium
[17] Namsoo Kim; Aparin, V.; Larson, L.E." A Resistively Degenerated Wideband Passive Mixer with Low Noise Figure and High IIP2," Microwave Theory and Techniques, IEEE Transactions, vol.58, no.4, pp.820-830, April 2010.
[18] Min Wang and Carlos E. Saavedra, "Reconfigurable Broadband Mixer with Variable Conversion Gain
Reconfigurable Broadband Mixer with Variable Conversion Gain" Microwave Symposium Digest (MTT), 2011 IEEE MTT-S International.
[19] Zhangf Liu , Jing Wang, "A Novel CMOS Reconfigurable Mixer for Dual-mode GNSS Receiver" Applied Mechanics and Materials Vols. 303-306 (2013) pp 1838-1841Trans Tech Publications, Switzerland.
[20] L. Chiu, T. Y. Yum Q. Xue and C. H Chan, "A High-Performed Sub-Harmonic Self-Oscillating Mixer for Modern Wireless Communication System" TENCON 2005 IEEE Region 10.
[21] Andrea Mazzanti, Mohammad B. Vahidfar, Marco Sosio, and Francesco Svelto, "A Low Phase- Noise Multi-Phase LO Generator for Wideband Demodulators Based on Reconfigurable Sub-Harmonic Mixers" IEEE Journal of Solid-State Circuits (Volume: 45, Issue: 10, Oct. 2010)
[22] Laleh Rabieirad and Saeed Mohammadi, "A Dual-Mode Programmable Distributed Amplifier/Mixer"Microwave Symposium Digest, 2009. MTT '09. IEEE MTT-S International.
[23] Mirko Pasca, Vincenzo Chironi, Stefano D'Amico, Marcello De Matteis, Andrea Baschirotto "A 12dBm IIP3 Reconfigurable Mixer for High/Low Band IR-UWB Receivers" PhD research in Microelectronics and Electronics (PRIME), 2013 9th conference.
[24] Y.Gao, F. Huang, L. Wu, and J. Cheng, "A Low-Power Reconfigurable Mixer for MB-OFDM UWB Receivers," in Microelectronics Electronics, 2009. Prime Asia 2009. Asia Pacific Conference on Postgraduate Research in, pp. 97–100, Jan
[25] D. Fu, L. Huang, H. Du, and H. Yuan, "A 0.18nm CMOS High Linearity Flat Conversion Gain Down-Conversion Mixer for UWB Receiver," in Solid-State and Integrated-Circuit Technology, 2008. ICSICT 2008. 9th International Conference on, pp. 1492–1495, Oct.
[26] K. Choi, D. H. Shin, and C. Yue, "A 1.2-V, 5.8-mW, Ultra-Wideband Folded Mixer in 0.13-μm CMOS," in Radio Frequency Integrated Circuits (RFIC) Symposium, 2007 IEEE, pp. 489–492, June.
[27] M. Brandolini, P. Rossi, D. Sanzogni, and F. Svelto, "A CMOS Direct Down-Converter With +78dBm Minimum IIP2 for 3G Cell-Phones," in Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International, pp. 320–601 Vol. 1, Feb
[28] D. Manstretta, M. Brandolini, and F. Svelto, "Second-Order Inter-modulation Mechanisms in CMOS Downconverters," Solid-State Circuits, IEEE Journal, vol. 38, no. 3, pp. 394–406, Mar 2003.
[29] A. Abidi, "General Relations between IP2, IP3, and Offsets in Differential Circuits and the Effects of Feedback," Microwave Theory and Techniques, IEEE Transactions on, vol. 51, no. 5, pp. 1610–1612, May. 2003.